Variable Bit-Rate Receiver for WDMA/WDM Systems

C.-S. Li, *Senior Member, IEEE,* F. Tong, *Senior Member, IEEE,* and G. Berkowitz

***Abstract*— We report the design, fabrication, and the characterization of a variable bit-rate receiver designed for wavelength-division multiplexing and wavelength division multiple access (WDM/WDMA) applications. The performances of these receivers can be optimized for bit-rates ranging from 300–1500 Mb/s. The tunability of the receiver bandwidth is achieved through adjusting the gate bias of a microFET used as an active feedback resistor in the transimpedance amplifier.**

***Index Terms*—Variable bit-rate receiver, WDM.**

I. Introduction

PROTOCOL transparency has become increasingly important in a heterogeneous networking environment in which network access units with different protocols and transmission rates have to be attached to the same network. This feature is particular applicable in optical networks using wavelength-division multiplexing (WDM) and wavelength division multiple access (WDMA) in which very high level of protocol transparency can be achieved. A 20-channel WDM system with quasiprotocol transparency has already been commercialized [1]. In this system, there are plug-in line cards and each card is prescribed to a specific protocol at a fixed bit rate.

For a system to support different protocols, the optical receiver at the receiving end node would ideally be able to adjust to the bit rates for different protocols. Lacking this variable bit-rate tunability, the receivers must then set to cover the highest possible data rate transmitted in the networks. For low data rates, the large receiver bandwidth inevitably results in a suboptimal sensitivity due to the excessive thermal noise.

One means to configure a receiver to operate in a range of bit rates with optimal performance is to vary the transimpedance of the amplifier. This can be achieved by tuning the gate voltage of a microFET, which is used to replace the feedback resistor in the transimpedance amplifier [2]. Because of their small parasitic capacitance, active feedback resistors can achieve wide-band nonintegrating response and stability against ringing and oscillation. In this letter, we discuss the design, implementation and the characterization of a variable bit-rate receiver designed particular for WDM/WDMA data communication systems.

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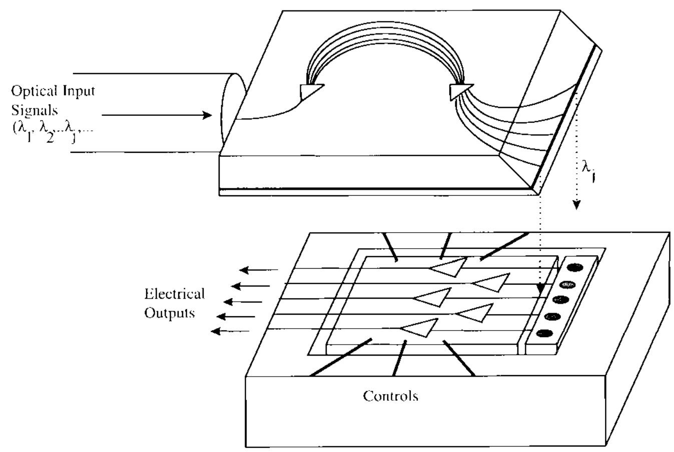

Fig. 1. Schematics showing the WDM receiver array consisting of an optical demultiplexer, detector array and a transimpedance amplifier array.

II. WDM Receiver Array and Protocol

Fig. 1 shows the schematics of our proposed WDM optical receiver array consisting of an optical demultiplexer (such as SiO_2 array waveguide grating [3]) and an InGaAs photodetector array connected to an array of GaAs transimpedance amplifiers with variable bit-rate capability. The optical demultiplexer spectrally resolves the input wavelengths and each of these wavelength channels can be directed onto its corresponding detector in the detector array through a total internal reflection at the end face of the demultiplexer [4], [5]. Signals from all wavelength channels will be received and amplified, and the bandwidth of each receiver can be adjusted by an external voltage in accordance to the incoming data rate. The detector array and the amplifier array can be packaged with high density interconnect (HDI) [6] which offers a levelled and planar surface such that direct coupling with the demultiplexer is practical. Several 32-channel tunable receiver modules for WDMA networks were packaged using similar technology [4], [5].

For the signaling protocol, we propose the bit rate information to be prescribed in the wavelength channel. Since the incoming data rates will not be changed frequently, the bit rate information can be carried in the prefix and recovered by a phase lock loop attached to each receiver. Once the bit-rate information is determined, the control voltage responsible for altering the receiver bandwidth is generated by a table

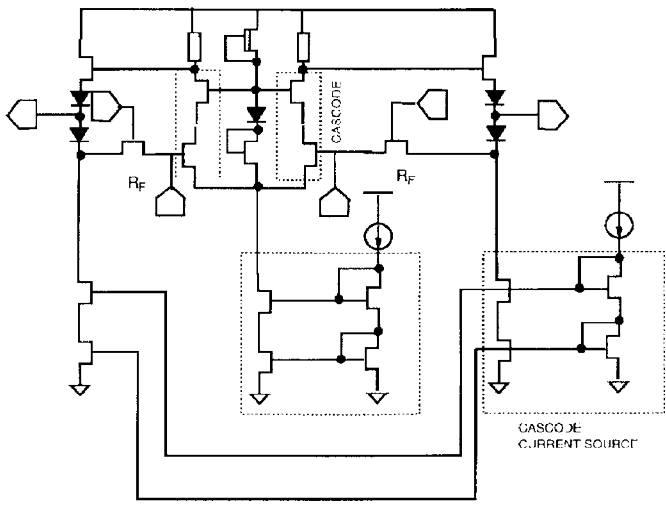

Fig. 2. Circuit diagram of the variable bit-rate receiver.

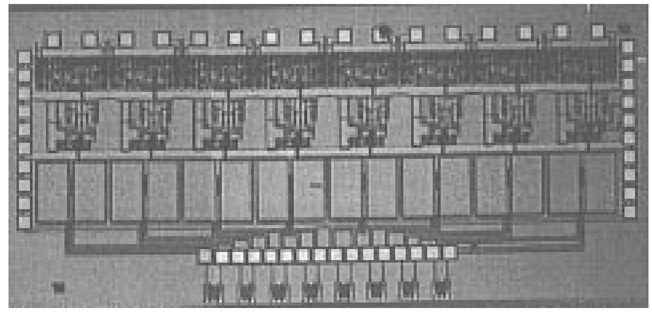

Fig. 3. Chip photograph of the eight-channel receiver array. The variable bit-rate receiver is the right-most receiver in the picture (receiver 8, the left-most receiver being receiver 1). The pads on top of the picture are for the signal output. The pads located on both sides are for controls, power and ground. The pads on the bottom are for connecting with the InGaAs detectors. The MSM detectors are located at the bottom of the picture.

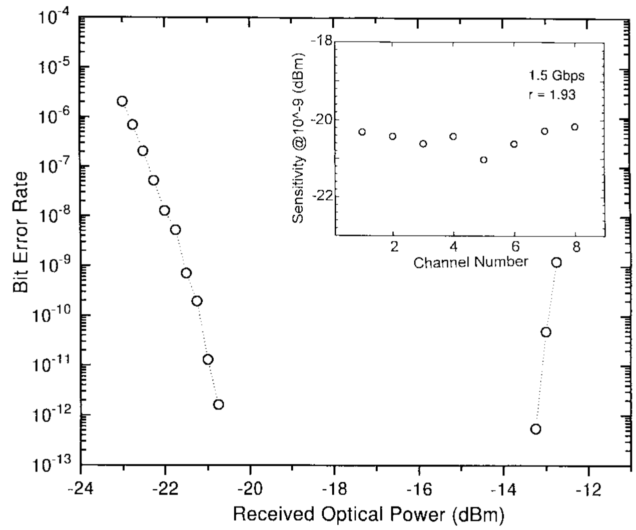

Fig. 4. BER measurements of receiver 4, the best receiver, at $\lambda = 0.85$ μm with MSM detector. Using a $2^7 - 1$ NRZ PRBS with an extinction ratio of 1.93, the inset shows the performance variation (at 10^{-9} BER and 1.5 Gb/s) of receivers in the array.

lookup and converted by a D/A operation. The data in each wavelength channel are then extracted by the timing/data recovery unit, which is connected to the receiver output.

III. Receiver Design

The circuit diagram is shown in Fig. 2. The transimpedance preamplifier has a cascode differential front-end followed by a source follower stage. The size of the input MESFET is optimized such that the noise is minimized. Both of the current sources for the differential pair at the front end and at the source follower are cascode configured to maximize gain bandwidth product. When operating in the regime of linear drain current I_d versus drain voltage V_d (as opposed to the saturation regime in the normal FET), the microFET can assume the role of feedback resistor $R_F (R_F = V_d/I_d)$ whose value depends on the applied gate source voltage $V_{\rm gs}$. I_d can be expressed as $I_d = (W/L)\mu_n C_i (V_{\rm gs} - V_t) V_d$ for $V_d \ll V_{\rm gs} - V_t$, where V_t is the threshold voltage, μ_n is the electron mobility, C_i is the capacitance per unit area, and W and L are the respective channel width and channel length of the FET. The ratio of V_d over I_d yields $R_F = (L/W)[\mu_n C_i (V_{\rm gs} - V_t) V_d]^{-1}$, showing that R_F can be controlled by $V_{\rm gs}$.

In our design, the output of the preamplifier is connected to a buffering stage to provide additional current gain to drive a 50-Ω transmission line.

IV. Fabrication and Experimental Results

The fabrication of the transimpedance amplifier utilizes a gate length of 1.2 μm with a transconductance g_m of 140 mS/mm, f_T of 15 GHz and combined $C_{\rm gs}$ (gate-source capacitance) and $C_{\rm gd}$ (gate–drain capacitance) of 500 fF. A microFET with identical W and L of 1.2 μm is used as an active feedback resistor with $V_{\rm gs}$ set by external voltages. Note that because of the differential front-end design, there is ac-coupling capacitors of 14.3 pF located at the inputs of the amplifiers. Due to these capacitors, the receiver requires the data to be lined coded by, for example, 8B/10B code to eliminate low frequency and dc components below 200 MHz. The amplifier array circuit consumes 150 mA with a +5 V. Both monolithically integrated MSM detectors and hybrid integrated InGaAs PIN detectors were used for characterization. The GaAs MSM detector has a diameter of 80 μm. The electrode width is 0.8 μm separated by a finger pitch of 2.5 μm, yielding a measured responsivity of 0.3 A/W at 0.85-μm wavelength. The InGaAs PIN detector has a diameter of 75 μm and a measured responsivity of 1.0 A/W at 1.55 μm.

Fig. 3 shows the photograph of the receiver array. As shown in the figure, each GaAs transimpedance amplifier is separated from its neighbor by 560 μm. Contact pads (250-μm pitch) were introduced to connect with the InGaAs detectors. The additional GaAs metal–semiconductor–metal (MSM) detectors (responsive at $\lambda = 0.85$ μm), each separated by 250 μm, were integrated with the receivers to simplify testing procedures. For testing at $\lambda = 1.55$ μm, the MSM detectors are removed by saw cut and wire bondings are used to connect the amplifiers with InGaAs detectors. Although an eight-channel transimpedance amplifier array was fabricated, only one amplifier (amplifier 8, rightmost amplifier) is im-

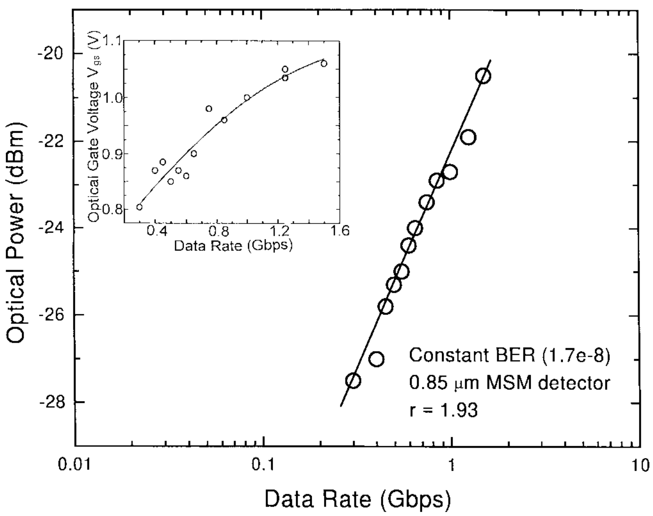

Fig. 5. Plot of required optical power to maintain a constant BER of 1.7 $\times$ 10^{-8} as a function of data rate. See text for details. The inset shows the measured optimal $V_{\rm gs}$ at different data rates.

plemented with variable bit-rate capability. The other seven array elements use passive feedback resistors in the usual transimpedance amplifier configuration so as to measure as many key array parameters from a single chip.

Bit-error-rate (BER) measurements were performed for bit rates ranging from 300 to 1500 Mb/s, using an extinction ratio of 1.93 and a $2^7 - 1$ NRZ PRBS at 0.85-μm wavelength. In the experiment, a multimode fiber (50 μm/125 μm) is used to butt-couple the laser light (from HP83404A) to the MSM detectors biasing at $+5$ V. Single mode fiber is used for the case of InGaAs detectors. The best receiver sensitivity is measured to be -21 dBm at 10^{-9} BER at 1.5 G/ps on receiver 4 at $\lambda = 0.85$ μm with the MSM detector, with a measured dynamic range of $\sim$7 dB (Fig. 4). There is little variation ($<$1 dB) among receivers in the array, as displayed by the plot of the sensitivity (at BER of 10^{-9}) as a function of receiver number in the inset. Small-signal modulation experiments show that the receiver 3-dB bandwidth is 0.79 GHz with the MSM detectors. Smaller receiver bandwidth (0.55 MHz) is measured with the InGaAs PIN detector array (3-dB bandwidth $\sim$1.5 GHz); the bandwidth degradation is attributed to the wire bonding and should not be a factor in the HDI packaging.

To demonstrate the bit-rate variable capability, we first determined at a given bit rate the optimal gate source voltage, $V_{\rm gs}$, applied to the microFET such that lowest BER is generated. In these measurements, the input optical power to the detectors was set at a level to produce a BER of $\sim 10^{-9}$ at $V_{\rm gs}$. These results are shown in the inset of Fig. 5. For a bit-rate range of 0.3 to 1.5 Gb/s, $V_{\rm gs}$ is found to vary proportionally from 0.8 to 1.07 V with the data rates. The as-obtained gate voltages can then be applied to the BER measurements for the corresponding data rates. Fig. 5 shows the results derived from a series of these BER experiments, plotting the required input optical power to maintain a constant BER (1.7×10^{-8}) over the tested data-rate range. The linear dependence suggests the bit-rate variable capability of the receiver. If the feedback resistance is the same for high bit-rates as well as for low bit rates, the optical power required to achieve identical BER should be similar, given equal contributed thermal noise in both cases.

V. Summary

In summary, we have demonstrated the feasibility of a variable bit-rate receiver particularly designed for WDM/WDMA systems. The tunability of the receiver bandwidth is achieved through adjusting the gate bias of a microFET used as an active feedback resistor in the transimpedance amplifier.

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